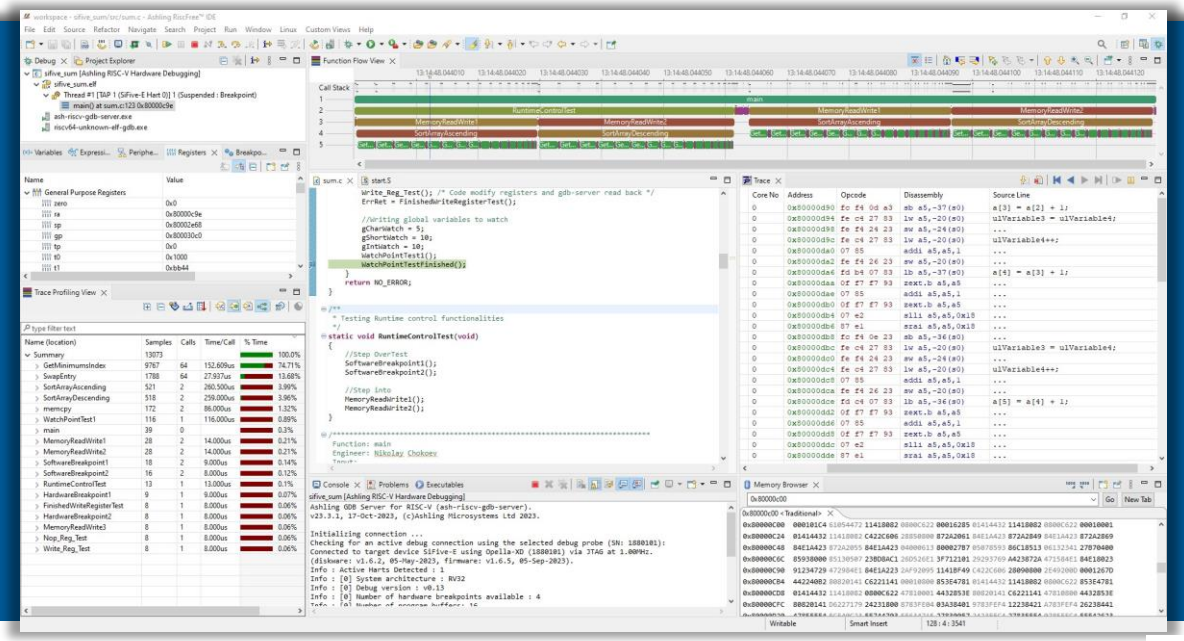
RiscFree™ SDK
IDE, Compiler and Debugger



RiscFree Features

- IDE with full source & project creation, editing, build & debug support.
- Works with Windows and Linux Hosts.
- ***RiscFree*** includes a single-shot installer that installs & automatically configures all the component tools to work "out-of-the-box".
- Automatic source-code formatting, syntax colouring and function folding.
- Integrated GCC and/or LLVM compiler toolchains.
- Project wizards, templates and examples.
- Ashling hardware debug & trace probe support is fully integrated into the ***RiscFree*** debugger allowing hardware-based debug & easy setup, capture & display of trace, profiling & analysis data.
- Integrated Code Coverage and Profiling support and views.
- Heterogeneous (e.g., Arm + RISC-V + ARC) & homogeneous debug & trace support for multi-core SoCs sharing a single debug interface (accessed via probe) is provided.
- On-chip and off-chip trace/debug analytics support.
- ROM or RAM based debugging support (e.g., hardware breakpoints for flash-based support).
- Integrated QEMU ISA simulator for 32-bit & 64-bit cores. Support for other industry standard instruction & cycle accurate simulators.
- High-level register viewer.
- Integrated RTOS (e.g., FreeRTOS or Zephyr) & OS (e.g., Linux) debug support.
- Creation of customisable ***RiscFree*** user-interface "Views" (Windows) using Python scripts.
- Fully scriptable debug interface using Python or GDB syntax.
- Support for SoC wide breakpoints i.e., a single breakpoint can halt all cores in active debug launches.
- Core dump debugging allows post-crash debugging and analysis using a core dump file.
- ***RiscFree*** supports core-specific software breakpoints in shared code i.e., only halt if a specified core is running for common code shared between multiple cores.
- ***RiscFree*** has a dedicated Global Variables view to browse and show global variables in the application (ELF).

Product	Order Code
RiscFree SDK (supports RISC-V, Arm and Synopsys ARC & ARC-V)	RF-GENERAL
RiscFree SDK (supports MIPS RISC-V ISA P8700 & I8500 CPUs with GCC toolchain)	RF-MIPS