Ashling's *RiscFree*™ Toolchain now supports Western Digital's SweRV EH2 and EL2 RISC-V Cores

July 9, 2020 – Redwood Shores, CA and Limerick, Ireland. Ashling a leading provider of embedded development tools announced today full tools support for the latest Western Digital's RISC-V open source SweRV EH2 and EL2 cores on their *RiscFree*™ Toolchain.

Western Digital's RISC-V open source SweRV now has two new additions EH2 and EL2 which are both available to the open-source community. EH2 is a high-performance 32-bit, dual-thread, superscalar, 9-stage pipeline core with simulated performance of up to 6.3 CoreMark/MHz and a footprint of 0.067 mm2 using TSMC's 16nm CMOS process technology. EL2 is a second-generation SweRV core aimed at medium-performance embedded applications. It is a 32-bit, single issue with a 4-stage pipeline with simulated performance of 3.6 CoreMark/MHz and supporting the RISC-V RV32IMC instruction set. SweRV2 offers compelling capabilities for embedded devices supporting data-intensive edge applications such as storage controllers and industrial IoT.

> "We are happy to extend our support for the RISC-V ecosystem by adding support for the SweRV EH2 and EL2 devices. Our customers have a production-grade RISC-V tools option supporting all RISC-V cores with Ashling support for any toolchain customization needed" said Hugh O'Keeffe, Ashling's Managing Director.

RiscFree™ is Ashling's Eclipse-based Integrated Development Environment (IDE) for RISC-V and provides a complete, seamless environment for RISC-V software development including a single-shot installer that installs and automatically configures all the component tools to work "out-of-the-box". Features include:

- IDE based on Eclipse with full source and project creation, editing, build and debug support
- RISC-V GNU/LLVM compiler toolchains including optional user specific customisations and support for both EH2 and EL2.
- Project wizards, templates and examples for RISC-V based devices from multiple vendors
- Fully integrated debug support including support for homogeneous and heterogeneous multi-core SoCs.
- Opella-XD for RISC-V JTAG Probe. Ashling's Opella-XD is a high-speed JTAG debug probe for embedded debug on RISC-V cores.

For more information, refer to: https://www.ashling.com/swerv/

About RISC-V
RISC-V open architecture ISA is under the governance of the RISC-V International. Visit https://riscv.org for more details

About Ashling
Ashling is a world-class technology partner offering integrated solutions, tools, and design services that are at the heart of the embedded environment. Through its close cooperation with leading semiconductor vendors, Ashling has become a leader in the Embedded Software Development Tools market. Its solutions are used by engineers across a diverse range of applications from automotive and aerospace to healthcare and IoT. Ashling's HQ and Engineering centre is in Limerick, Ireland. Ashling has sales and support representatives worldwide. For more information on Ashling see: www.ashling.com.

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