

## Ashling announce *RiscFree*<sup>™</sup> support for MachineWare’s SIM-V RISC-V Instruction Set Simulator.

Limerick, Ireland. 29<sup>th</sup> May 2023.

Ashling announced today that Ashling’s *RiscFree* SDK now provides target debug support for MachineWare’s **SIM-V** RISC-V Instruction Set Simulator.

*RiscFree* is Ashling’s SDK including an IDE, compiler, libraries and debugger and provides software development and debug support for RISC-V. Since its introduction, Ashling’s *RiscFree* SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace have made it the go-to choice for 32-bit and 64-bit RISC-V software development.

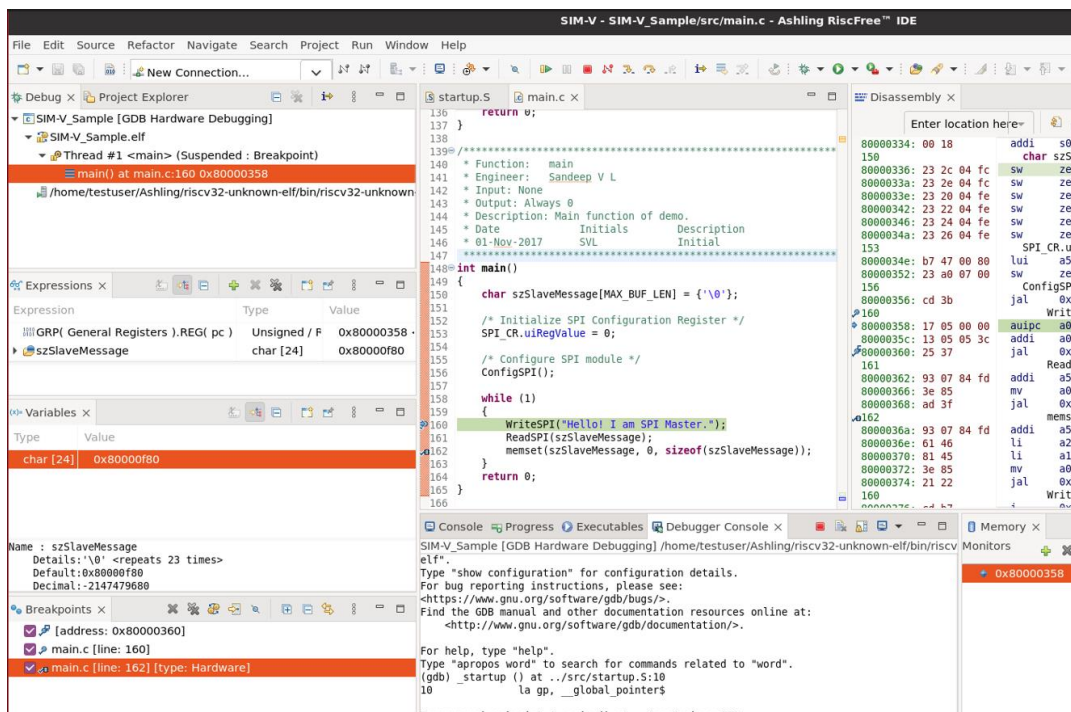
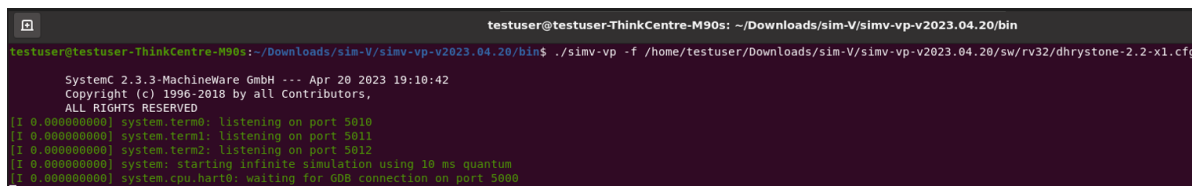


Figure1. *RiscFree* connected to MachineWare SIM-V

“We are excited to offer our customers target debug support for the MachineWare SIM-V simulator” said **Hugh O’Keeffe, CEO of Ashling**. “This collaboration between Ashling and MachineWare enables developers to accelerate their RISC-V software development, testing, and debugging, ultimately leading to faster time-to-market for RISC-V-based products.”

MachineWare's **SIM-V** is a RISC-V simulator that enables developers to test and verify RISC-V based systems and software applications. The simulator provides a high-performance Instruction Set Simulator (ISS) that supports all RISC-V standard extensions, including privileged ISA and custom instructions. The intuitive **SIM-V** extension allows quick addition of custom instructions and registers to **SIM-V** to get immediate feedback on design choices.



```
testuser@testuser-ThinkCentre-M90s: ~/Downloads/sim-V/simv-vp-v2023.04.20/bin
testuser@testuser-ThinkCentre-M90s:~/Downloads/sim-V/simv-vp-v2023.04.20/bin$ ./simv-vp -f /home/testuser/Downloads/sim-V/simv-vp-v2023.04.20/sw/rv32/dhrystone-2.2-x1.cfg

SystemC 2.3.3-MachineWare GmbH --- Apr 20 2023 19:10:42
Copyright (c) 1996-2018 by all Contributors,
ALL RIGHTS RESERVED
[1 0.00000000] system.term0: listening on port 5010
[1 0.00000000] system.term1: listening on port 5011
[1 0.00000000] system.term2: listening on port 5012
[1 0.00000000] system: starting infinite simulation using 10 ns quantum
[1 0.00000000] system.cpu.hart0: waiting for GDB connection on port 5000
```

**Figure2. Invoking MachineWare SIM-V.**

*“MachineWare is excited to work with Ashling to bring this solution to the RISC-V community” said **Lukas Jünger, Managing Director with MachineWare.** “The combination of Ashling’s RiscFree SDK and MachineWare’s SIM-V simulator provides developers with a powerful and flexible solution for simulation-based RISC-V software development, enabling them to develop high-quality applications more efficiently and begin target debug before hardware availability.”*

Ashling’s **RiscFree** SDK with support for the **SIM-V** simulator is now available and for more information, please visit the Ashling website at <https://www.ashling.com/ashling-riscv/> for more on our RISC-V tools.

### **About Ashling**

Ashling have been a leading provider of Embedded Development Tools & Services since 1982 with design centres in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East and America. Visit [www.ashling.com](http://www.ashling.com) for more general details.

### **About MachineWare**

Founded in 2022 in Aachen, Germany, MachineWare leverages decades of experience in system level simulation and high-performance simulation tooling. Visit <https://www.machineware.de/> for more details.

### **About RISC-V**

The RISC-V open architecture ISA is under the governance of RISC-V International. Visit <https://riscv.org> for more details.

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