MIPS chooses Ashling's RiscFree™ Toolchain for its RISC-V ISA compatible IP cores

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SILICON VALLEY, CA, USA. Ashling and MIPS announced today that Ashling's ***RiscFree™*** Toolchain has been extended to support MIPS RISC-V ISA based IP cores. ***RiscFree™*** is Ashling's Integrated Development Environment (IDE) including a compiler and debugger for RISC-V based development, and it now has support for MIPS RISC-V ISA based IP cores, enhanced by MIPS' own proven and tested Core Framework Platform.

> *"We are delighted to have Ashling **RiscFree™** support for our RISC-V ISA IP cores. Our engineering teams have worked closely together developing the toolchain in parallel with the core IP and believe this can result in rapid time-to-market for our end customers,"* said **Don Smith, Vice President of Engineering at MIPS**.

The Ashling ***RiscFree™*** toolchain will include support for both code development and debug on MIPS RISC-V IP cores and includes advanced features such as multi-core and multi-cluster support, Linux debug awareness, real-time trace support, and cache awareness. It also comes with a range of Ashling hardware probes supporting debug and trace. In addition, a targeted and optimised GCC toolchain is included and fully integrated into the ***RiscFree™*** IDE.

> *"We are excited to see MIPS, one of the first companies to bring a RISC based architecture to the market back in the 1980s, now expanding to offer RISC-V ISA compliant cores. We've a long history of working together and believe the support of our market-leading **RiscFree™** Toolchain will help in the rapid market adoption of their MIPS RISC-V ISA cores,"* said **Hugh O'Keeffe, CEO of Ashling**.

For more information on Ashling's ***RiscFree™*** see: https://www.ashling.com/ashling-riscv/ and for more information on MIPS see: www.mips.com.

About Ashling

Ashling have been a leading provider of Embedded Development Tools & Services since 1982 with design centres in Limerick Ireland and Cochin India and sales and support offices in Europe, Asia Pacific, the Middle East and America. We have over thirty years' experience in developing tools for embedded systems engineers including high-speed Debug and Trace Probes supporting a broad range of MCUs, SoCs and Soft (FPGA) based designs. Our software tools include IDEs, Debuggers, Compilers and Simulators and we support all the main embedded architectures including ARC, Arm, MIPS, Power Architecture and RISC-V through our ***RiscFree™*** platform. We have a particular focus on RISC-V and are the first company to bring tools to the market supporting heterogenous debug of RISC-V cores along with cores from other vendors. Visit www.ashling.com for more details.

About MIPS

MIPS is a leading developer of highly scalable RISC processor IP for high-end automotive, computing and communications applications. With its deep engineering expertise, an ecosystem built over 35 years and billions of MIPS-based chips shipped to-date, today the company is accelerating RISC-V innovation for a new era of heterogeneous processing. The company's proven solutions are uniquely configurable, enabling semiconductor companies to hit exacting performance and power requirements and differentiate their devices. Visit: www.mips.com

About RISC-V

The RISC-V open architecture ISA is under the governance of the RISC-V International. Visit https://riscv.org for more details.

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